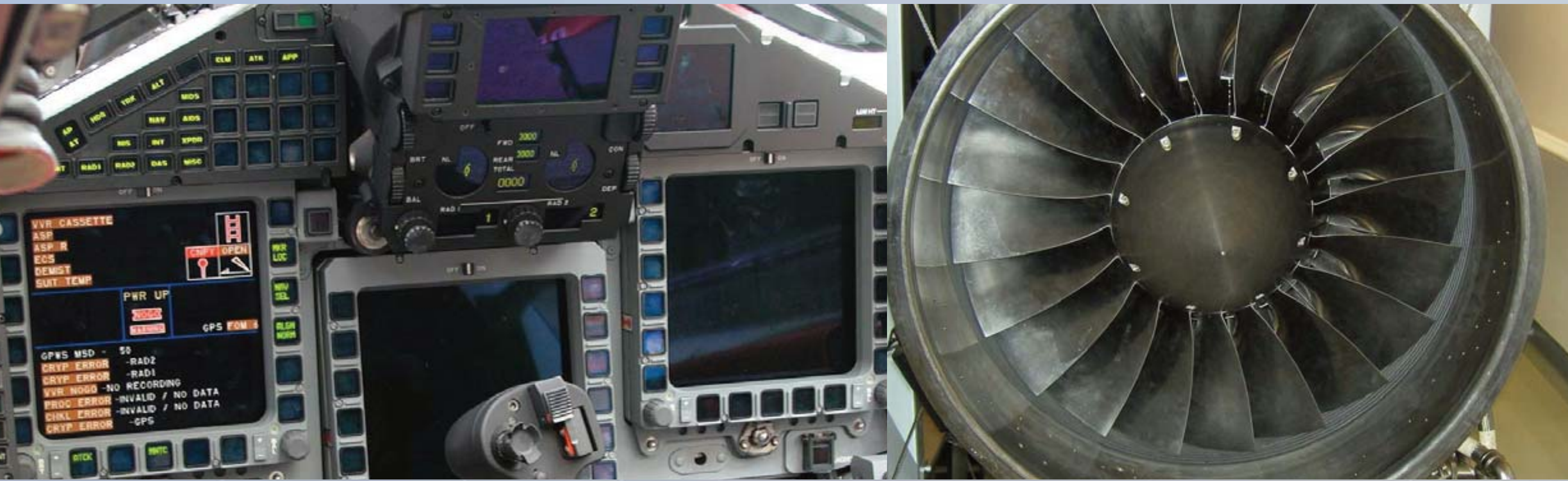
VALID LINE

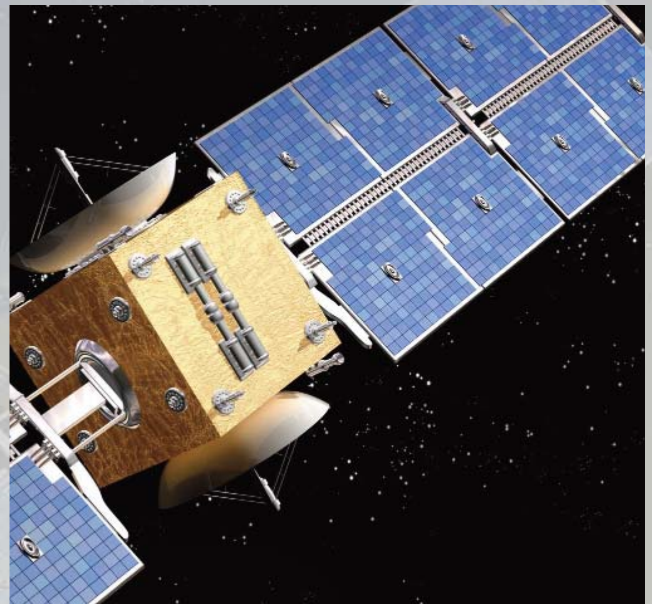
Functional test platform

HIGH-PERFORMANCE



Choosing a functional test solution means that it must satisfy (at least) three fundamental requirements:

- The solution should meet present and future performance needs
- The solution should retain the ability to adequately mimic features of old, to-be-replaced equipment.
- The solution should include comprehensive hardware and software tools and yet be fully open to COTS (Commercial Off-The-Shelf) hardware and software.



The **Valid Line** is the ultimate integrated functional test solution, capable of meeting and exceeding these requirements for analog, digital and mixed-signal testing, both at board level (SRA/SRU) and box level (LRA/LRU), in the factory and in the field.

The **Valid Line** benefits from Seica's unrivalled experience in testing complex types of electronic boards and assemblies, featuring advanced DSP and FPGA-driven digital technology and a comprehensive set of test generation, debug and diagnostic proven solutions.

The **Valid Line** has a proven track record of successfully replacing obsolete functional test equipment, from GR179X to GR275X, from L200 to L300, from S720 to S790 and custom STE for box level test and validation.

Offering the best test-oriented stimulus and measurement dedicated hardware, the Valid Line can readily be extended to incorporate GPIB, LXI and VXI COTS solutions. Operating under a powerful test-oriented environment (VIVA), the system can also be fully directed by other test sequencers, like N.I. TestStand or Agilent VeePRO, and/or combine use of a variety of programming languages like C++, VBS, and programming environments like LabWindows/CVI, LabView, and others.

FACTORY AND DEPOT SRU/LRU FUNCTIONAL ATE

VERSATILE TEST ARCHITECTURE

At the heart of the system is the VIP test backplane. Controlled by the system PC through the high-speed fiber-optic bus, the VIP test backplane hosts channel cards, routing cards and internal instrumentation. The VIP test backplane offers unrivalled flexibility, with full connection to the test receiver, ample room for expansion, built-in signal and power buses to accommodate all requirements of stimuli and measurement distribution to the UUT (Unit Under Test).

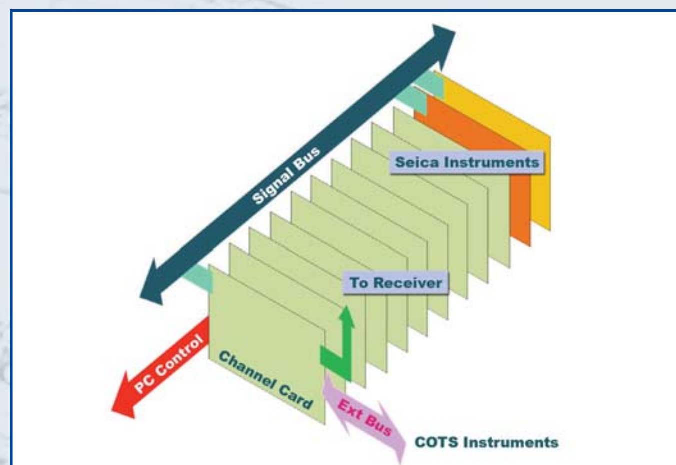
The Valid Line can be provided with a traditional SEICA, Mac-ODU or Virginia Panel VP12 Receivers. Custom solutions using other technologies (i.e. to retain existing fixtures) are also available. All solutions offer a system capacity of up to 1,024 channels, which can be doubled by adding a second test backplane.

Latest generation of F50 digital channel cards offer each 32 channels with 25MHz dynamic performance, local timing phases and windows, local multiple level references, parallel and serial operating mode. Each channel provides dynamically high speed stimuli and responses, with large backing memory and algorithmic capabilities. Other channels' features include CRC, pulse generation control, POD functionalities for 1149.2 applications, direct time and frequency measurement. Flexible control assures Legacy Replacement of obsolete equipment as well as easy and direct coping with bus-testing, serial-mode testing, IEEE 1149.2 and other protocols.

F50 cards include analog switching on each channel to be mated, at fixture level or in the system, with analog channel cards, thus offering full hybrid digital/analog capability.

Analog channel cards offer a unique 3D architecture which allows COTS instruments to be directly connected through eight external bnc I/Os. Routing can then be local with independent clusters of 32 channels, or system-wide through the 8-line analog bus of the VIP test backplane. This unique architecture can easily cope with test scenarios requiring a large number of analog stimuli to be applied simultaneously to the UUT.

If high current stimuli need to be switched, other channel cards are available, with dual connection to the analog bus or to the separate power bus.



FLEXIBLE TEST-ORIENTED INSTRUMENTATION

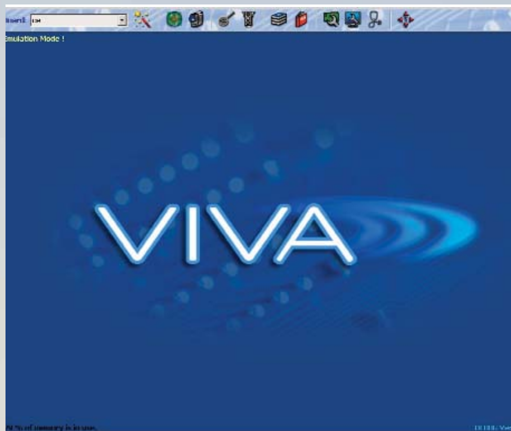
The main analog test resource is based around the ACL subset, which provides multiple, DSP-driven AC/DC stimuli and measurement automatically routed to all channels, to reproduce the required test scenario and to provide fast and accurate results.

Automotive, aerospace and industrial applications often require providing parallel test of to the UUT, with several different analog stimuli applied and synchronized measurements taken. An example of this is the case of SRU or LRU interfacing sensors or driving tools. Such situations are impossible to reproduce on conventional ATE without the addition of complex active electronics on the fixture. Not so with the iFUN parallel test solution offered in the Valid Line. The iFUN hosts 16 independent, DC-programmable analog channels; if required, the iFUN can mount up to eight additional resources, in any combination out of the currently available AWG and Digitizer modules. Multiple iFUN modules can be installed in the system, thus responding to the most exotic SRU/LRU test needs.

Whenever needed, the system offers ample capacity to add external GPIB, VXI or LXI instruments to meet RF, HV or load specifications,

For high performance digital, to best serve military contractual requirements, the Valid Line can also be configured with the Talon T964 Digital Resource Modules. Fully integrated in the test generation, run-time and diagnostic environment of the Valid Line, the Talon T964 cards provide ultimate digital test performance at 50MHz with 1nsec edge placement resolution and tester per pin architecture.

POWERFUL TEST GENERATION, VALIDATION, RUN-TIME ENVIRONMENT



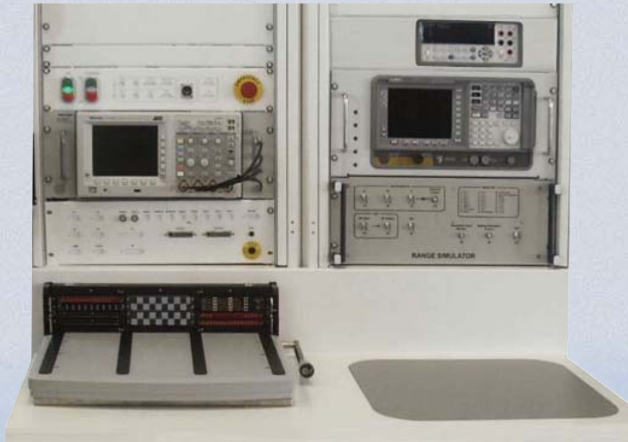
As are all Seica systems, the Valid Line is based on the powerful VIVA software environment. CAD data can be directly imported to create a comprehensive data base for test generation, validation and diagnostics. The board schematic, layout and nomenclature are dynamically linked and controllable by the user.
Test steps and source code are also synchronized during execution to ease debug.
VIVA also includes a number of tools specifically oriented for functional test generation such as a simulator for digital test, a Virtual Channel encoder for 1149.2 cluster test, and a powerful, hardware-independent test language (NVL). All of these features enable the test engineer to completely focus on achieving the desired results, rather than on resolving limitations of the software environment.
The complete software architecture of the Valid Line is based around the Component Object Model (COM) technology, which enables the creation of re-usable software components, easily linkable, to favour a powerful open system environment. Thus, the Valid Line systems can be delivered to operate in the environment which is familiar to the customer, such as N.I. TestStand or Agilent VEE. Through the use of COM technology, either VIVA or N.I. TestStand communicate directly with object codes, passing events and data at test execution time. Instrumentation and test sequences can be readily operated under COTS tools, such as Microsoft Visual C++ or Visual Basic, N.I. LabWindows/CVI or LabView, and others.
Besides full access to the Virtual Instrument tools offered with COTS instruments, the Valid Line offers QuickTest, a global Virtual Instrument environment, to access all Seica hardware. QuickTest allows the user to graphically interact in real time' with the tester hardware and the UUT to create test sequences that can be prepared off-line (hardware emulation) or directly executed and viewed.
Results can be stored and become part of the overall test program. QuickTest allows technicians to use any part of the powerful and complex platform of the Valid Line with the same ease that they use any familiar lab instrument, without requiring knowledge of the system and time-consuming data base preparation.

COMPREHENSIVE DIAGNOSTIC TOOLS

Level III test requirements demand precise fault location in order to speed up operations, reduce the cost of PCB repair and eliminate scrap. The Valid Line fully supports guided probe operations for digital and analog type of circuits as well as fault dictionary based techniques.
Digital guided probe at speed can be driven by simulated, or directly learned data. A fault dictionary can also be used on line, in conjunction with the guided probe, or off line. In addition to the proprietary simulation tools, the Valid Line can also directly post-process LASAR simulation results.
Analog diagnostics extend the guided probe algorithms to analog clusters, with analog DC and AC measurements and automatic trace back and isolation of the source of the fault.

LOW COST MODULAR, COST EFFECTIVE SYSTEM CONFIGURATION AND ERGONOMICS

With the Valid Line you are not locked into a single system configuration. The base system is offered on a vertical architecture, combining a prestigious looking line with a high degree of ergonomics essential for operator comfort. The system includes an ample work/desk area and a flat, adjustable LCD monitor. The main diagnostic instruments (manual measurement probes, oscilloscopes, transducers) are strategically located above the test adapter section.
The System bay can be supplied in the traditional Seica extra-size, or with the standard 19” dimensions.
If the main utilisation of the system is with bed-of-nails fixtures, a horizontal work-bench version is offered. In both cases, expansions are easily accommodated by adding a second or third bay to host additional instrumentation.



Optimum scalability of the system is ensured by means of plug-in expansions and upgrades directly in the field.
A version of the Valid, hosted on the ATEC-MT series, is supplied through EADS Test and Services, in partnership with Seica.

DECADES OF DEFENCE AND AEROSPACE TEST EXPERIENCE

Since its creation in 1986, Seica has gained recognition as a trusted supplier of test equipment and services for defence and aerospace electronics manufacturers and depots worldwide. All over the world Seica products and services help ensure cost-controlled Legacy Replacement of obsolete ATE, mission readiness of critical modules, manufacturing and logistics preparation for future advanced electronics.
Seica’s hardware, software and service approach has made the Valid Line the natural choice to replace obsolete ATE at Thales, Dassault Aviation, Galileo Avionica, GE, offering smooth migration and long-term support of existing TPS’s, and state-of-the-art tools for future developments on avionics such as the Eurofighter Typhoon or the Rafale.
Continuous technical innovation is driven concurrently by the large presence of Seica’s solutions on the commercial market, such as the automotive industry, where Seica has a prominent position, and Seica’s unique philosophy of using a “common” hardware and software core for all of its products benefits all Seica customers.
The addition of new test technology for one industry is immediately available to others: one example is Boundary Scan 1149.2 test generation and diagnostics, which is now present in the Seica platform as a natural extension of functional test executed on clusters combining physical and virtual access, and not only as a separate, external tool.
Combining test experience and direct research and development investment with an open hardware and software approach, Seica offers unconstrained but comprehensive solutions to its customers. As an example of the appreciation of the quality of Seica test environment, VIVA has been chosen by EADS North America to provide comprehensive test development and execution software for their Talon Instruments™ family of T964™ high-performance digital test instruments.

THE VALID LINE

Designed around a common hardware and software architecture, the Valid Line is offered in several different configurations to address for the customer; ergonomics, test strategy, and deployment from board depot to full production level test.

VALIDATE AND VALID PLUS BOARD TEST SYSTEMS FOR LEVEL III

VALIDATE

ValidATE is the architectural implementation of the Valid Line for Level III (Board Test) applications. The system bay measures 60x96x182 cm and hosts 28 card cage slots using a VIP Test Backplane for a capacity up to 768 digital (or 384 full hybrids) high performance functional channels. Channel capacity can be doubled by adding a second VIP Backplane; a larger version of the system, hosting a 40 slot VIP Backplane(s) is also available. The system is offered with a standard choice of two types of receivers, the Seica traditional pin-bed and the ODU, which has a wide variety of extensions for ancillary connections of high frequency signals, coax, fiber-optics, pneumatic, etc. Custom receivers to accommodate specific requirements are also readily engineered. The system can be expanded to accommodate one or two additional bays for external instrumentation.

VALIDATE PLUS

ValidATE Plus is electrically the same as the ValidATE System. The ergonomics are changed to best suit the requirements of combined in-circuit and functional test, when a bed-of-nails fixture is more appropriate. Together with the ability to thoroughly verify the functionality of digital, analog and mixed-mode circuitry, the ValidATE Plus can extend its application to power-off, structural and power-on in-circuit techniques. The system combines best-in class solutions for board testing to meet performance, capacity and fault location capabilities. The system takes advantage of all techniques to reduce test generation cost, without affecting fault coverage or throughput. Power-off structural tests, using both junction and capacitive techniques, are first used to isolate simple manufacturing faults. Power-on in-circuit tests, both analog and digital, including extensions to IEEE 1149 techniques, are then deployed through the non-multiplexed hybrid channels of the system. Where required, fast On Board Programming (OBP) operations can be performed. Finally, the full power of functional test can certify operation of the UUT.
The ValidATE Plus base configuration is a single horizontal bay that accommodates the system's power distribution, UUT power supplies and the test backplane to host various types of channel cards and instrumentation. The ValidATE Plus is an ideal ergonomic solution to be used with bed-of-nails fixtures, offering the operator full access control to the UUT, control panel, oscilloscope and system's PC, as well as a comfortable area for documentation, schematic and tools. The system can be expanded to accommodate one or two additional bays for external instrumentation. Standard or custom fixtures are pneumatically (or alternatively vacuum) engaged into a robust, high performance receiver, granting access through the signal bus of the test backplane to all resources of the system.

LEVEL II: LOW COST MODULAR ARCHITECTURE

Special to Type Test System (STTE) integrators have justified their choice based on cost advantages potentially offered by targeting the solution on the specific end product requirements, as opposed to the more general but more expensive General Purpose ATE (GPATE). In trying to accomodate the multiple requirements of hundreds of LRU that can be part of a final system, from serial to parallel digital, from LF to RF, from Optronics to Pneumatic, the cost of instrument, routing and interfacing often exceed budget limitations. Furthermore, the need to respond to multiple logistic environments, Factory, Depot or even sheltered in the field, adds to the complexity, hence to the initial and long term cost of the GPATE solution. Leaner, more agile compact and cost controlled solutions are therefore offered by STTE, with the added attractive of in-house possible realisation. But this is at the expense of limited, unflexible architectures. This also generates a proliferation of different ATE. And the overall cost, if measured on the life of the product, adding documentation, support, adaptations and re-engineering, obsolescence, ends up to be much more than what expected.
The purpose of Seica's Low Cost Modular ATE (LCMA) is to offer the capability, performance and flexibility of GPATE with the agility, scalability and cost control that can make it competitive to a wide range of STTE solutions.
The CORE of the Seica's LCMA is based on Valid LF and Digital stimuli/masurement instrumentation and routing, offering high performance and large capacity to meet parallel LRU Test Requirements. Proprietary hardware is combined with GPIB, VXI, PXI or PCI Plug-and-Play COTS instruments as required, for digital serial and HF LRU requirements. Signal routing architectures provide a three dimensional way to connect both internal and external instrumentation at a glance.
For best signal integrity stimuli and responses are connected to the fixture and then to the UUT using highperformance receivers like Virginia Panel VP12.
The system offers the ability to be fully controlled under the powerful VIVA Test Environment, to elect instead for other COTS Test Environments (like NI TestStand, or HP VEE) or to combine the best of the two under control of SuperVIVA.
The result is a system offering performance, flexibility and capacityty of GPATE, within a scalable architcture and overal cost of ownership competitive with STTE products. LCMA allows to create, around a CORE of proved hardware and software, a proven solution to meet AUDIO, VIDEO, RF, OPTRONICS or PNEUMATIC LRU test requirements.

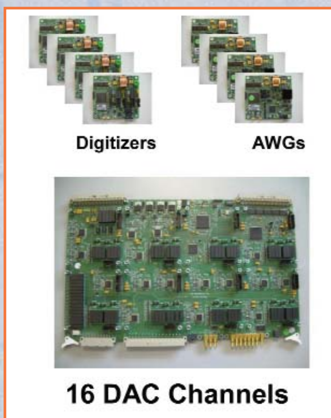
LEVEL I

VALID PTE

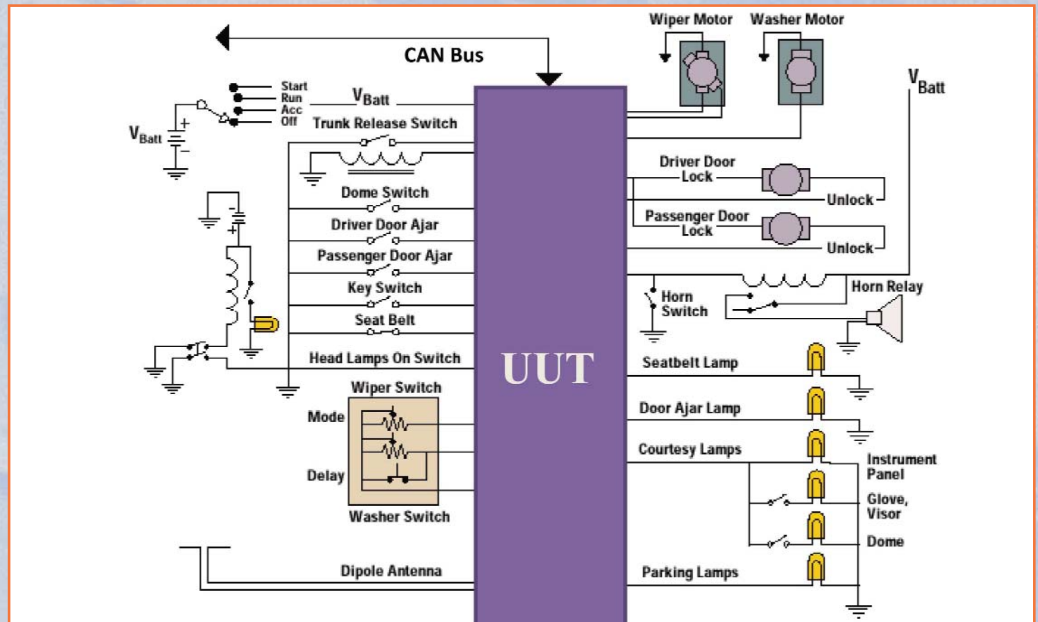
The PTE-100 Portable Test Equipment is a powerful, flexible and transportable Intelligent Break Out Box designed to provide checkout, test and troubleshooting for critical parts of transportation electronic systems. The PTE-100 offers test personnel direct access to electrical signals for probing, voltage injection, isolation checks, voltage/current and time/frequency measurements. It offers the ability to analyze HOT and LOADED circuits, verifying missing, corrupted or valid signals. Electrical verification activities become more efficient, repeatable and safe, thanks to the introduction of software controlled test sequences that reduce human error and guide diagnostic routines. Using the same advanced instrumentation of the Valid Line, the PTE-100 can be configured to control up to 256 connections. The front panel, which can be customized to specific applications, offers two lines of connectors (A and B) where the (normally connected) unit under test can be split and routed. The PTE-100,inserted between the split parts, allows hot connection and disconnection operations, signal measurements and signal injections. Each pin of the line A or B has access to an independent 4-line bus (8 lines when connected together) going to the stimulus/measurement unit of the system (the ACL unit). Up to 256 channels can be configured, with 500V/2A carrying voltage/current and 30VDC/200VAC/2A hot switching. Test generation and run time are controlled via the powerful QuickTest environment, which is suited for two main modes of operation: as an instrument or as an automatic tester. The interactive display of the stimulus/measurement/connection scenario offers menu-driven programming, direct execution, and oscilloscope visualisation of each of the test operations. While in instrument mode, the user has full, immediate, direct control of each step by step action; the automatic mode allows storage of the sequence of operations into a series of instructions, which can be modified or enriched, and used for self-documentation or executed by non-skilled operators. Without limiting flexibility, the system includes robust, customizable rules-driven procedures to avoid damaging the unit under test or the PTE-100 itself.
Housed in a 590x285x430mm chassis, and weighing approximately 20 kg,, makes it easy to transport in a carrying case. The PTE-100 is ideally suited for Level 1 applications in commercial and military programs for avionics, ships and transportation.

REAL TIME TEST EMULATION

When UUTs are part of complex systems, the ATE will be able to emulate the operating conditions by applying multiple stimuli and making multiple measurements in parallel. The iFUN is an analog test card designed to fulfil these requirements of real-time signal generation and measurement at functional test. The card includes 16 four quadrant, grounded DC voltage generators, programmable up to 20V with 16 bit resolution. The DC generators allow simultaneous application of independent signals at the inputs of the UUT, to precisely reproduce discrete signals coming, for example, from sensors that are part of the system, as frequently encountered in automotive, defence, aerospace, and industrial applications. The card can also mount up to eight additional, independent test modules, either Arbitrary Waveform Generators (AWG) or Digitizers, in any combination, to extend operations to a real parallel test scenario. Each AWG module has four floating voltage generators, with programmable current limiting, and 16 bit resolution. Generation is through DDS (Direct Digital Synthesis) technique and supported by 2M word of memory. The Digitizers allow simultaneous synchronized measurement as required by real-time test, featuring floating mode with 16 bit resolution and up to 50MS/s sample frequency. The Valid system can hold up to four iFUN boards, thus offering virtually unlimited parallel test capability in a matrix-free architecture.

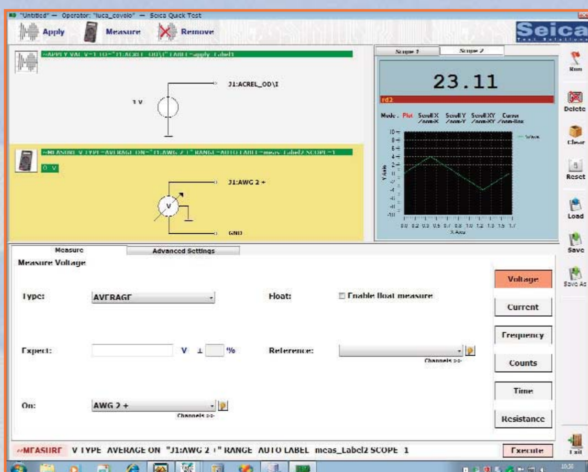


Our iFUN Solution



Your Test Problem

QUICK TEST



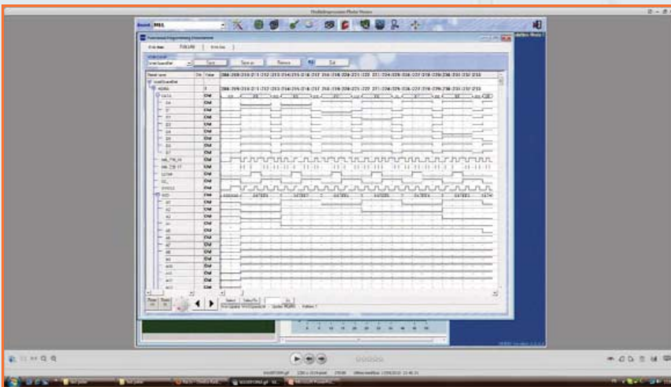
The figure below shows the main operating screen of Quick Test. In the upper left-hand corner, the system displays the connection(s) being made. The upper right-hand corner serves to have oscilloscope displays of the measurements made. The bottom part of the screen is to modify the parameters of the measurement; Tin the bottom line, the system directly creates the correspondent language statement to the action graphically executed.

Quick Test has been developed to offer engineers the ability to combine the power of an ATE with the simplicity of a hand held instrument. With direct graphical access to the complete path from the instrumentation to the UUT, Quick Test allows preparing and executing functional test scenarios in minimal time, without knowledge of the architecture of the resources and the intricacies of language to be used. With the test specification in one hand, the user will transfer the information directly into the graphical environment of Quick Test and, at a glance, get it executed and display the results.
Quick Test is easy to manipulate and to experiment with assisting the engineer or technician in verifying test proposals.
Quick Test can be used like a Lab Instrument, for example, prior to starting to prepare complex test procedures or as an interactive diagnostic tool to confirm the location of a fault. The tremendous flexibility of Quick Test makes it an ideal compliment to the Level 1 Portable Test Equipment, but also very beneficial as a tool for Level 2 STE integrators, or as a common tool between test engineers and design engineers for the preparation of Level 3 board test programs.
Quick Test gives direct access to connections between instrumentation and the UUT, and also supports a solid rules based control scenario, which warns the user of potential dangerous operations to protect the system and the UUT. Individual test operations, once created and accepted, can be automatically converted on equivalent language statements and stored for automatic documentation or later re-execution.

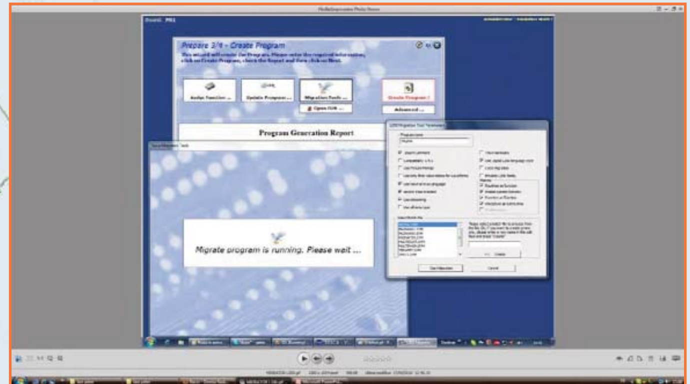
LEGACY REPLACEMENT

Seica can safely claim to have the most experience on Legacy Replacement of obsolete ATE, inclusive of the replacement solution, the tools for TPS migration and the service to provide turn-key solutions. From the old GR179X/GR2750,Computer Automation (CA) Marathon, and S79X test systems, to the more recent L3XX systems, Seica has successfully served customers worldwide to migrate thousands of test programs, assuring life extension to long term defense products. There are several reasons to make Seica the preferred partner, and the Valid Line the preferred solution, for Legacy Replacement:

- Since the start of the company in 1984, development of TPS for defense customers has been a key activity for Seica engineers.
- The Valid Line architecture is scalable to reproduce the most sophisticated digital and analog ATE configurations.
- The digital, analog, routing capabilities of the Valid Line match and exceed those of the ATE to be replaced.
- The Valid Line is committed to invest in new technologies, while at the same time retaining legacy techniques, like wide range digital logic levels (+/- 30V),, guided probe diagnostics and fault dictionary, and analog guided probe routines, etc.
- The Valid Line can be provided with the same receiver used on the ATE to be replaced, thus accepting old fixtures without any signal degradation.
- The Legacy Replacement environment of the Valid Line, which includes a wide number of input paths from most common functional ATEs, is designed to fully automate TPS migration, with minimal user intervention, without loss of coverage and with comparable, self documenting program structure.

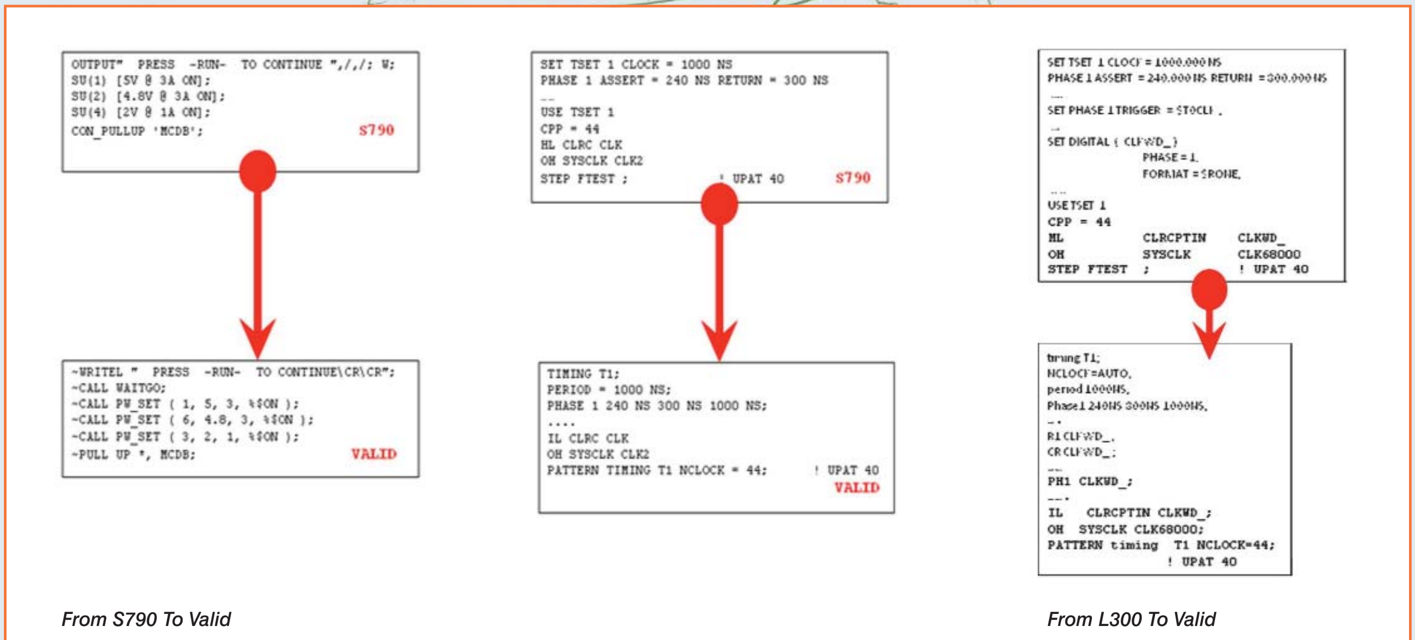


Legacy Replacement Logic Analyzer



Legacy Replacement Environment

The figure below shows the correspondence between the original L300 instructions and the correspondent translation for execution by the Valid hardware. The translation environment allows selecting different formats for the Valid language so that not only the characteristics and performance of the test action are maintained, but also the readability is optimal, should some corrections be required at verification. The translator operates with the same accuracy to convert the diagnostic data files; the translator for L300 also covers conversion of the analog tests and associated routing.



From S790 To Valid

From L300 To Valid

OPEN SOFTWARE ENVIRONMENT

All Seica instruments are fully supported by COM libraries to allow direct integration with external environments, such as NI TestStand or Agilent VEE, and can be programmed by external languages or graphic tools. Similarly, the Seica test environment can call directly and execute software objects developed within external test engines like LabView, LabWindows CVI, etc. This architecture allows the user the advantages of years of experience embedded in Seica's products and the flexibility to take advantage of other commercial products as well.
For example, allowing customers the freedom to use the most suitable test sequencer, test language, or graphic tool.

The figure below shows one of the instruments of the ACL card, controlled within LabView.

Seica Quick Test
Seica VIVA
NI TestStand
Agilent VEE
Seica .PAT
NI LabVIEW
NI LabWindows/CVI

Seica A P E
SeicaNVL
Seica VL
NI TestStand Engine
NI LabVIEW
NI LabWindows/CVI
Seica MMPWT Toolkit

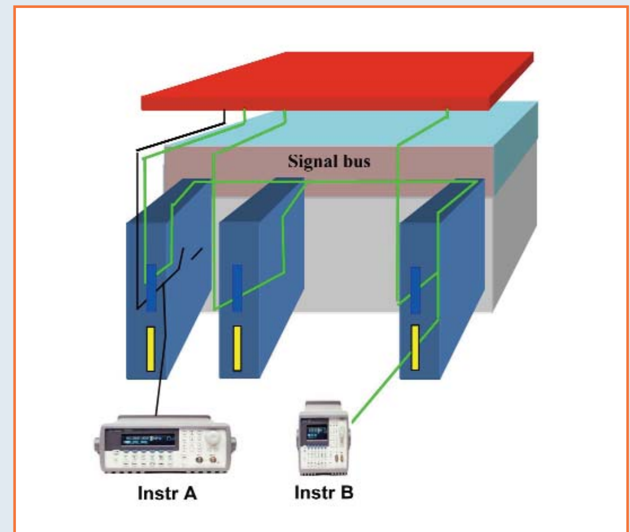
Seica Hardware Drivers
Device Driver (LCPORTIO) / TCP-IP / USB
"External" Hardware Drivers
NI Drivers / IVI Drivers / ...

Seica Hardware
"External" Hardware

The following block diagram shows the diversity, flexibility, and interconnection of the software modules within the Valid Line.

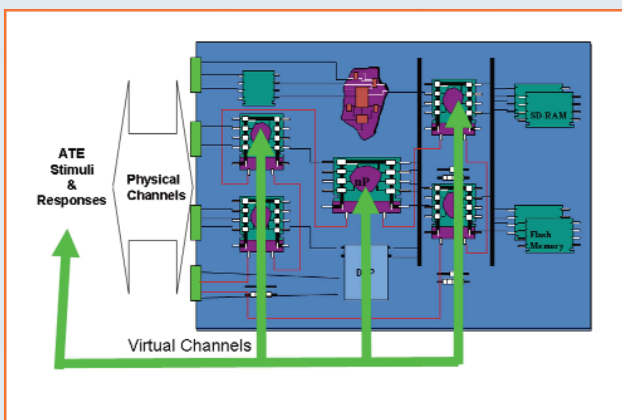
ROUTING ARCHITECTURE

Routing signals from instrumentation to the UUT has always been the bottleneck for the test system. An easy solution is, of course, to bring all signals from instrumentation to the receiver, and then assure switching and connections on the fixture; but at what cost! Most ATE solutions have an internal signal bus, where instruments connect through instrument switching cards, as well as separate switching channel cards going to the UUT. To limit space required by the matrix relays, complex multiplexing solutions are often used. Instead, the Valid Line uses a more flexible 3D routing architecture that avoids multiplexing limitations, relies on an eight lines signal bus, and yet allows simultaneous connection of a larger number of stimuli and measurements to the UUT. This is accomplished by the S64A module, a 3D scanner matrix card, used to switch the internal/external ATE instrumentation to the receiver. The card contains 32x8 groups of reed relays able to connect the eight lines of the signal bus to any of the 32 channels going to the ATE receiver and to the UUT. The unique architecture of the card also allows connection to eight external channels (extended bus), available on dedicated coaxial connectors. External instrumentation can be routed through the card, allowing either local or global connections. In local mode, the card creates a cluster matrix, 8x32, between the instruments connected to the card and its 32 channels, isolated from the rest of the system. In global mode, the instruments are also connected to the signal bus, becoming available to every channel of the system. A combination of local and global bus connections through multiple cards allows having a large number of different analog stimuli to be applied and measured during the same test scenario. These features are particularly valued when board testing legacy replacement solutions are offered, or for STE integrators of second level test equipment.



In the figure below, instrument A is actually connected on a local mode to pin(s) of the first channel card, while instrument B is connected on global mode and available to all channels of the system.

FUNCTIONAL TEST WITH JTAG



The VBN Test Strategy

Despite that almost twenty years have passed since the initial introduction of JTAG 1149 testability standard, very little, or no advances, have been made in combination with functional testers. The technology has given rise to a variety of dedicated test systems, focused on structural fault detection of components that are boundary scan compliant and included in JTAG cells on the unit under test. Use of JTAG has also been extended by encapsulating the technique into ICT or Flying Probe test systems in order to increase the structural fault coverage. Functional test has not yet taken advantage of this technology, and has therefore continued to struggle with high cost of test program generation, due to the increase of components complexity and lack of control and observation points on UUT. Fortunately, this issue has been recently addressed on the Valid Line, with the introduction of an innovative test generation technique, called VBN, for Virtual Bed of Nails. With VBN, the user is encouraged to segment the UUT into clusters of components that offer easier test generation and can be accessed via a combination of physical pins and virtual pins, where the latter are pins connected to a JTAG chain. All that is required is to declare those pins as Virtual Channels, and to describe to the system the BSDL (boundary scan description language) for each JTAG component and the JTAG interconnection path within the netlist of the board. The programmer can now prepare his/her test program “as if physical and virtual channels were the same.” Once this is done, the tester will automatically convert the parallel test program into the appropriate mixture of parallel and JTAG TAP vectors and generate them as required. The test results and diagnostic results will also be displayed to the user consistently with this cluster test approach. VBN allows functional test to take advantage of the presence of JTAG components on the UUT and reflect it into reduced test generation cost, increased fault coverage and diagnostic resolution.

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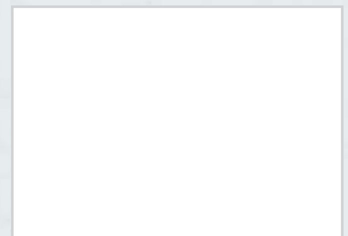

Seica reserves the right to change the technical specifications without notice